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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,259	04/20/2001	Paul F. Struhsaker	WEST14-00021	1533

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EXAMINER	
PEZZLO, JOHN	
ART UNIT	**PAPER NUMBER**
2662	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/839,259	STRUHSAKER ET AL.	
	Examiner	Art Unit	
	John Pezzlo	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/23/01, 1/10/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

I. Claims 1-36 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Each of the independent claims, 1, 11, and 24, cite the following element "a control preventing the memory segments from receiving changes to the data elements contained therein at a rate faster than a transfer rate of memory segments over the data link". This element has no support in the specification, the abstract, or the drawings. Therefore, one of skill in the art will be unable to understand and implement the invention with no knowledge in the documents to aid the skilled artisan even with the aid of experimenting, since one of skill in the art has no idea of how to interpret the claim element.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

II. Claims 1-36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

1. Each of the independent claims, 1, 11, and 24, cite the following element "a control preventing the memory segments from receiving changes to the data elements contained therein at a rate faster than a transfer rate of memory segments over the data link". This element is confusing since there is no mention about whether the changes to the memory segment are prevented while the memory segment is being transferred or just the rate of transfer is less than the rate of change of the memory segment. It appears this element has no relationship to transferring memory segments while changes to the memory segments are occurring except for the rate of changing memory segments versus the rate of the transmission of the data link. It seems that some synchronization of the changes made to the memory and the transfer of that memory over the data link is in order to prevent corrupted data from being transferred as well as matching the rates of changes made to the memory and the transfer rate over the data link.

2. Claims 10, 22, 35 cite the data link comprises an ATM switch. This is confusing since a data link is not a switch but a pathway for conducting the transmission of electronic signals. (The examiner assumes an ATM protocol link.)

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

III. Claims 1-3, 6-8, 11-13, 16-18, 21, 23-26, 29-31, and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Alaiwan et al. (EP 0 441 087 A1) hereinafter Alaiwan.

1. Regarding claim 1 – Alaiwan discloses a memory (memory, 14-1 in Figure 1) containing data elements each stored within one plurality of defined memory segments, wherein the data elements within the memory segments may be selectively changed, refer to Figure 1, call out 14-1, and page 5 lines 10 to 16.

Alaiwan discloses a direct memory access circuit (memory change detector) (memory change detector, 28-1 in Figure 1) capable of automatically copying memory segments from the memory to a queue, Alaiwan discloses that the memory change detector captures the memory elements which have changed in register, 60-1 in Figure 2 (queue), refer to Figures 1 and 2 and page 5 lines 49 to 51 and page 6 lines 45 to 58.

Alaiwan discloses a data link (mirror bus, callout 34 in Figure 1 and state data, callout 40-1 in Figure 1) coupled to the queue, wherein each of the plurality of memory segments is structured to form a data packet which may be transmitted without internal changes over the data link, Alaiwan discloses that the memory change detector through the bus driver transmits the memory changes over the mirror bus (callout 34 in Figure 1 and state data, callout 40-1 in Figure 1) to the write ahead queue (WAQ) callout 32-2 in Figure 1, refer to page 5 lines 49 to 55.

Alaiwan discloses a control (finite state machine) preventing the memory segments from receiving changes to the data elements contained therein at rate faster than a transfer rate of memory segments over the data link, refer to page 7 lines 50 to 52.

2. Regarding claims 2 and 12 and 25 – Alaiwan discloses a processor (callout 12-1 in Figure 1) intermittently changing data elements within the memory segments (memory, callout 14-1 in

Figure 1), wherein the data link operates without direct control by the processor, refer to page 5 lines 52 to 54.

3. Regarding claims 3 and 13 and 26 – Alaiwan discloses a set of memory segments mapping to a corresponding set of memory segments (register, 60-1 in Figure 2) within a device coupled to the data link, refer to Figures 1 and 2 and page 5 lines 49 to 55 and page 6 lines 45 to 58.

4. Regarding claims 6 and 16 and 29 – Alaiwan discloses wherein the direct memory access circuit (memory change detector, callout 28-1 in Figure 1) copies memory segments containing changed data elements therein from the memory to the queue (register, callout 60-1 in Figure 2), the copying of memory segment being triggered by a processor (callout 12 – in Figure 1), which intermittently changes data elements within the memory segments, refer to Figures 1 and 2 and page 5 lines 49 to 55 and page 6 lines 45 to 58.

5. Regarding claims 7 and 17 and 30 – Alaiwan discloses wherein the processor writes a direct memory access descriptor for a memory segment containing a changed data element and sets controls bits initiating copying of the memory segment by the direct memory access circuit (memory change record generator, callout 58-1, in Figure 2), refer to Figure 2 and page 6 lines 45 to 58.

6. Regarding claims 8 and 18 and 31 – Alaiwan discloses wherein the direct memory access circuit (memory change record generator, callout 58-1, in Figure 2) copies memory segments containing changed data elements therein from the memory to the queue (register 60-1, in Figure 2), the copying of a memory segment being triggered by a circuit monitoring writes to preselected memory addresses to detect changes to a data element within any memory segment, refer to Figure 2 and page 6 lines 45 to 58.

7. Regarding claim 11 – Alaiwan discloses an active component, refer to Figure 1, callout 12-1, processor.

Alaiwan discloses a standby component, refer to Figure 1, callout 12-2, processor.

Alaiwan discloses a system for memory equalization between the active and a standby components comprising: counterpart memories within the active and standby components each containing data elements stored within one of a plurality of defined memory segments mapped to addresses within both of the counterpart memories, wherein the data elements within the memory segments may be selectively changed, refer to Figures 1 and 2 and page 5 line 5 to page 6 line 30.

Alaiwan discloses a direct memory access circuit within each the active and standby components, the direct memory access circuit within the active component capable of automatically copying memory segments from the memory within the active component to a queue within the active component and the direct memory access circuit within the standby component capable of automatically copying memory segments from a queue within the standby component to the memory within the standby component, Alaiwan discloses that the memory

change detector through the bus driver transmits the memory changes over the mirror bus (callout 34 in Figure 1 and state data, callout 40-1 in Figure 1) to the write ahead queue (WAQ) callout 32-2 in Figure 1, refer to page 5 lines 49 to 55.

Alaiwan discloses a data link coupling to the queue within the active component to the queue within the standby component, wherein each of the plurality of memory segments is structured to form a data packet, which may be transmitted without internal changes over the data link, Alaiwan discloses that the memory change detector through the bus driver transmits the memory changes over the mirror bus (callout 34 in Figure 1 and state data, callout 40-1 in Figure 1) to the write ahead queue (WAQ) callout 32-2 in Figure 1, refer to page 5 lines 49 to 55.

Alaiwan discloses a control within the active component preventing the memory segments within the memory in the active component from receiving changes to the data elements contained therein at a rate faster than a transfer rate of memory segments over the data link, refer to page 7 lines 50 to 52.

8. Regarding claims 23 and 36 – Alaiwan discloses wherein the active component is one of N active components supported by the standby component, refer to Figure 8 and page 10 line 12 to page 11 line 26.

9. Regarding claim 24 – Alaiwan discloses selectively changing data elements each stored within one of a plurality of defined memory segments contained within a memory, refer to Figures 1 and 2 and page 5 line 5 to page 6 line 30.

Alaiwan discloses automatically copying segments from the memory to a queue utilizing a direct memory access circuit, Alaiwan discloses that the memory change detector through the bus driver transmits the memory changes over the mirror bus (callout 34 in Figure 1 and state data, callout 40-1 in Figure 1) to the write ahead queue (WAQ) callout 32-2 in Figure 1, refer to page 5 lines 49 to 55.

Alaiwan discloses transferring memory segments over a data link coupled to the queue, wherein each of the plurality of memory segments is structured to form a data packet which may be transmitted without internal changes over the data link, Alaiwan discloses that the memory change detector through the bus driver transmits the memory changes over the mirror bus (callout 34 in Figure 1 and state data, callout 40-1 in Figure 1) to the write ahead queue (WAQ) callout 32-2 in Figure 1, refer to page 5 lines 49 to 55.

inhibiting the memory segments from receiving changes to the data elements contained therein at a rate faster than a transfer rate of memory segments over the data link, refer to page 7 lines 50 to 52.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

IV. Claims 20, 33, and 34 and 9, 19, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alaiwan (same as above) in view of Nagar et al., "Issues in Designing and Implementing a Scalable Virtual Interface Architecture", IEEE, 2000, pages 405-412 hereinafter Nagar.

1. Regarding claims 20 and 33 – Alaiwan does not explicitly wherein a controller disclose for the data link within the standby component verifies data integrity for data packets received over the data link and acknowledges successful transfer of data packets over the data link to the active component.

Nagar teaches acknowledging successful transfers of memory changes from the active system to the backup system, refer to page 406 section 3.1 "Work and Completion Queues".

At the time of the invention it would have been obvious for a person of ordinary skill in the art to combine Alaiwan with Nagar to provide acknowledgements for successful transfer of data packets over the data link to the active component. The suggestion/motivation for doing so would have been that Alaiwan discloses the establish recovery point (ERP) process to recover from a fault in the active processor therefore providing the acknowledgements for successful transfers would make the system more robust with a higher quality and tolerance to failures and recoveries.

2. Regarding claim 34 – Alaiwan discloses receiving the memory segments in a queue within the standby component, wherein a direct memory access circuit within the standby component automatically moves memory segments from the queue within standby component

into a corresponding memory location in a memory within the standby component, refer to Figure 1 and 2 and page 5 line 5 to page 6 line 30.

3. Regarding claims 9, 19, and 32 – Alaiwan does not explicitly disclose wherein the direct memory access circuit sequentially copies each of the memory segments from the memory to the queue in a continuous loop.

Nagar discloses a continuous loop for completing memory transfers across a bus, refer to Figures 1 and 2 and page 408 section 4.2 "Messaging Sequence".

At the time of the invention it would have been obvious for a person of ordinary skill in the art to combine Alaiwan with Nagar to provide a continuous loop for transferring memory segments from the active memory to the backup memory. The suggestion/motivation for doing so would have been that Alaiwan discloses the establish recovery point (ERP) process to recover from a fault in the active processor therefore having a continuous loop would be an optimum method for keeping the backup system current with active system.

V. Claims 4, 14, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alaiwan (same as above) in view of Anderson, "FireWire System Architecture", second edition, IEEE 1394a, PC System Architecture Series, 1999, pages 13-16 hereinafter Anderson.

1. Regarding claims 4, 14, and 27 – Alaiwan does not expressly discloses wherein the memory further comprises a portion of Firewire Global Memory and wherein the data link comprises a Firewire data link.

Anderson teaches the use of Firewire Global Memory and Firewire data link, refer to pages 13-16.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Alaiwan with Anderson to provide a portion of the memory in Firewire Global memory and a Firewire data link. The suggestion/motivation for doing so would have been that Alaiwan discloses the requirements for the memory and the data link (refer to page 6 lines 31 to 41) and the Firewire architecture meets the requirements using standards which would be compatible with other equipment and make development less risky and faster saving time and money.

VI. Claims 5, 15, and 28 and 10, 22, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alaiwan (same as above) in view of the prior art cited on pages 7-15 of the specification.

1. Regarding claim 5, 15, and 28 – Alaiwan does not expressly disclose call state information for a call being processed, resource allocation records for resources allocated to a call being processed, and other information regarding a call being processed.

The prior art discloses using a redundant system to provide call state information for a call being processed, resource allocation records for resources allocated to a call being processed, and other information regarding a call being processed.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Alaiwan with the prior art to provide a call processing system with

redundancy. The suggestion/motivation for doing so would have been that a call processing system needs to be robust to process data and Alaiwan discloses a data processing system which is failsafe and recovers automatically from faults. The benefit being higher quality for the customers.

2. Regarding claims 10, 22, and 35 – Alaiwan does not expressly disclose wherein the data link comprises an asynchronous transfer mode (protocol link) switch.

The prior art discloses that the link could be an ATM protocol link.

At the time of the invention, it would have been obvious for an ordinary person of skill in the art to combine Alaiwan with the prior art to provide an ATM protocol link between the active and backup systems. The suggestion/motivation being that Alaiwan discloses the requirements for the data link (refer to page 6 lines 31 to 41) and the ATM protocol link meets the requirements using standards which would be compatible with other equipment and make development less risky and faster saving time and money.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Fung et al. (US 6,243,778 B1) discloses a transaction interface for a data communication system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Pezzlo whose telephone number is (571) 272-3090. The examiner can normally be reached on Monday to Friday from 8:30 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou, can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2600.

Any response to this action should be mailed to:

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or faxed to:

(703) 872-9306

For informal or draft communications, please label "PROPOSED" or "DRAFT"

Hand delivered responses should be brought to:

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John Pezzlo

6 July 2005

JOHN PEZZLO
PRIMARY EXAMINER